What is claimed is:

1. A structure for electrical testing during the manufacturing of a DRAM integrated circuit comprising:

a first region on a silicon substrate designated for a functional section of said integrated circuit;

a second region on a silicon substrate designated for said structure;

first semiconductor devices formed in said first, said semiconductor devices comprising first words lines in addition to first activating bit lines in addition to first non-activating bit lines;

second semiconductor devices formed in said second region, said semiconductor devices comprising second word lines in addition to second bit lines, said second word lines patterned over said semiconductor devices in a layout identical to that of first word lines in said first region, said second bit lines provided in a repetitive sequence of four bit lines each sequence comprising an activating bit line, a dummy bit line, a non-activating bit line and a dummy bit line, said second word lines patterned in said second region over said semiconductor devices in a layout identical to that of first word lines in said first region, said second bit lines being exposed bit lines in a pattern that is perpendicular with a pattern of said first bit lines;

a first contact pad formed at the ends of a plurality of said first and second word lines;

a second contact pad formed at the ends of a plurality of said activating first bit lines of said first semiconductor devices;

a first probe pad connected to said non-activating bit lines provided to first semiconductor devices formed in said first region; and

a second probe pad connected to said non-activating bit lines provided to second semiconductor devices formed in said second region.

2. The structure of claim 1 wherein said testing is testing of electrical shorts between capacitors of said DRAM integrated circuit, said testing further differentiating between first electrical shorts occurring between capacitors in a direction that is parallel with bit lines created in said first region on a silicon substrate and second electrical shorts occurring between capacitors in a direction under an angle with bit lines created in said first region on a silicon substrate.

3. The structure of claim 1 wherein said first region on a silicon substrate designated for a functional section of said integrated circuit and said second region on a silicon substrate

designated for said structure each comprise between about 50 and 5000 partially processed DRAM cells.

4. The structure of claim 1 wherein an array of capacitors forming part of said DRAM semiconductor devices comprises between about 1 and 100 columns and between about 1 and 100 rows.

5. The structure of claim 5 wherein said DRAM integrated circuit is a DRAM cell and said functional section is a portion of a cell array.

6. The structure of claim 5 wherein said cell array contains between about 50 and 5000 partially processed cells.

7. The structure of claim 5 wherein said DRAM integrated circuits are self-aligned polysilicon MOSFET devices.

8. A method of electrical testing of a test structure during the manufacturing of an integrated circuit, comprising the steps of:

(a) providing a test structure having

(i) a first region on a silicon substrate designated for a functional section of said integrated circuit;

(ii) a second region on a silicon substrate designated for said structure;

(iii) first semiconductor devices formed in said first region, said semiconductor devices comprising first words lines in addition to first activating bit lines in addition to first non-activating bit lines;

(iv) second semiconductor devices formed in said second region, said semiconductor devices comprising second word lines in addition to second bit lines, said second word lines patterned over said semiconductor devices in a layout identical to that of first word lines in said first region, said second bit lines provided in a repetitive sequence of four bit lines each sequence comprising an activating bit line, a dummy bit line, a non-activating bit line and a dummy bit line, said second word lines patterned in said second region over said semiconductor devices in a layout identical to that of first word lines in said first region, said second bit lines being exposed bit lines in a pattern that is perpendicular with a pattern of said first bit lines;

(v) a first contact pad formed at the ends of a plurality of said first and second word lines;

(vi) a second contact pad formed at the ends of a plurality of said activating first bit lines of said first semiconductor devices and selected second bit lines said second semiconductor devices;

(vii) a first probe pad connected to said non-activating bit lines provided to first semiconductor devices formed in said first region; and

(viii) a second probe pad connected to said non-activating bit lines provided to second semiconductor devices formed in said second region;

(b) mounting said silicon substrate in a probe testing station;

(c) supplying voltages to said contact pads;

(d) applying test probes to said probe pads; and

(e) measuring current flow through said test probes.

9. The method of claim 8 wherein a voltage of 2.0 volts is applied to said first contact pad.

10. The method of claim 8 wherein a voltage of 2.5 volts is applied to said second contact pad.

11. The method of claim 8 wherein a voltage of - 1.0 volts is applied to said third contact pad.

12. The method of claim 8 wherein said probe pads comprise said first probe pad.

13. The method of claim 8 wherein said probe pads comprise said second probe pad.

14. The method of claim 9 wherein current measured flowing through said first probe pad comprises current flowing between capacitances forming part of said DRAM integrated circuit in a diagonal direction, indicating diagonal bridging between capacitors of said DRAM integrated circuit.

15. The method of claim 13 wherein current measured flowing through said second probe pad comprises current flowing between capacitances forming part of said DRAM integrated circuit in a horizontal direction, indicating horizontal bridging between capacitors of said DRAM integrated circuit.

16. The method of claim 8 wherein said first region on a silicon substrate designated for a functional section of said integrated circuit and said second region on a silicon substrate designated for said structure each comprise between about 50 and 5000 partially processed DRAM cells.

17. The method of claim 8 wherein an array of capacitors forming part of said DRAM semiconductor devices comprises between about 1 and 100 columns and between about 1 and 100 rows.

18. The method of claim 8 wherein said integrated circuit is DRAM cell and said functional section is a portion of a cell array.

19. The method of claim 18 wherein said cell array contains between about 50 and 5000 partially processed cells.

20. The method of claim 18 wherein said integrated circuits are self-aligned polysilicon MOSFET devices.